IN THE CLAIMS

Per the revised amendment practice, a complete listing of all claims in the application follows.

Claims 1-21 (Cancelled).

22. (Original) A method of providing oxide for an in-process semiconductor device, comprising:

depositing a first oxide over said in-process semiconductor device; and

non-conformally depositing a porous second oxide onto said first oxide.

23. (Original) The method in claim 22, wherein said step of depositing a first oxide comprises depositing said first oxide in a chamber; and wherein said step of non-conformally depositing a porous second oxide comprises depositing said second oxide in said chamber.

24. (Original) The method in claim 22, wherein said step of non-conformally depositing a porous second oxide comprises reacting methylsilane with hydrogen peroxide.

25. (Original) The method in claim 22, wherein said step of non-conformally depositing a porous second oxide comprises reacting H_3SiCH_3 with H_2O_2.

26. (Original) The method in claim 25, wherein said step of non-conformally depositing a porous second oxide further comprises:

cooling said in-process semiconductor device to about 0°C before said reacting step; and

providing a temperature of about 450°C inside said chamber after said reacting step.

27. (Original) The method in claim 26, wherein said step of depositing a first oxide comprises reacting silane with hydrogen peroxide.

28. (Original) A method of providing a doped oxide, comprising:

flowing an oxide precursor over a portion of a semiconductor device;

forming an oxide from said precursor; and

subsequently annealing said oxide in an atmosphere containing a dopant.

29. (Original) The method in claim 28, wherein said annealing step comprises annealing said oxide in an atmosphere consisting of a selection of PH_3, a phosphate, a phosphite, NF_3, F_2, C_2H_6, trimethyl silane, CH_4, NH_3, B_2H_6, and combinations thereof.

30. (Original) The method in claim 29, wherein said annealing step further comprises annealing at a temperature ranging from 400 to 800°C, at a pressure ranging from 0.5 to 760 Torr, and for a time ranging from 10 seconds to 5 minutes.

31. (Original) A method of processing a surface of an in-process memory device, comprising:

providing said surface as part of said memory device using a non-CVD process;

flowing a material onto said surface;

turning said material into a first oxide; and

doping said first oxide.

32. (Original) The method in claim 31, wherein said step of providing said surface comprises providing a barrier oxide using a Flowfill process; and wherein said method further comprises blocking diffusion of a dopant from said first oxide using said barrier oxide.

33. (Original) The method in claim 32, wherein said step of doping said first oxide comprises:

doping a first portion of said first oxide with a first impurity; and

doping a second portion of said first oxide with a second impurity.

34. (Original) A method of providing an etch stop for a semiconductor device, comprising:

providing at least one support surface as part of said semiconductor device, said

surface having a horizontal portion and a non-horizontal portion;

depositing an oxide onto said support surface, wherein said oxide has a uniform thickness on said horizontal portion and a variable thickness on said non-horizontal portion; and

doping said oxide.

35. (Original) The method in claim 34, wherein said depositing step comprises depositing said oxide by way of a CVD process.

36. (Original) The method in claim 35, wherein said depositing step comprises depositing said oxide by way of an HDP CVD process.

37. (Original) A method of providing a CMP stop for a semiconductor device, comprising:

providing an element of said semiconductor device, said element having a top and a side;

depositing an oxide over said element, wherein said depositing leaves more of said oxide on said top than on said side; and

annealing said oxide in a doping atmosphere.

38. (Original) The method in claim 37, wherein said step of depositing an oxide comprises:

flowing a precursor to said oxide over said element; and

heating said precursor.

39. (Original) The method of claim 38, wherein said step of depositing an oxide comprises depositing said oxide using a spin-on-glass process.

40. (Original) A method of selectively doping a circuit device material, comprising:

depositing an oxide over a first horizontal surface of said circuit device material to the exclusion of a vertical surface of said material;

introducing a dopant into said oxide; and

diffusing said dopant from said oxide into said material.

41. (Original) The method in claim 40, further comprising a step of depositing a diffusion barrier over a second horizontal surface of said material; and wherein said step of depositing an oxide further comprises depositing said oxide over said diffusion barrier.

42. (Original) A method of filling a trench included as part of a semiconductor device, comprising:

reacting methylsilane with hydrogen peroxide in a chamber containing said semiconductor device;

allowing a product from a reaction of said methylsilane and said hydrogen peroxide to at least fill said trench;

changing said product into a silicon oxide; and

heating said silicon oxide in a boron atmosphere.

Claims 43-58 (Cancelled).

59. (Original) A method of forming oxide over a transistor gate and over a substrate extending laterally from under said gate, said method comprising:

forming an undoped first oxide over said gate and said substrate;

forming an undoped second oxide over said first oxide;

doping said second oxide after forming said second oxide;

depositing insulation over said second oxide after doping said second oxide;

initiating a removal of a portion of said insulation; and

stopping said removal with said second oxide.

60. (Original) The method in claim 59, wherein said step of forming an undoped first oxide comprises forming a TEOS-based oxide.

61. (Original) The method in claim 59, wherein said step of forming an undoped first oxide comprises forming a continuous silicon dioxide layer.

62. (Original) The method in claim 59, wherein said step of forming an undoped first oxide comprises forming a first oxide that is thicker over said gate than lateral to said gate, and wherein said first oxide is thicker over said substrate than lateral to said gate.

63. (Original) The method in claim 62, wherein said step of forming an undoped first oxide comprises forming a non-porous first oxide.

64. (Original) The method in claim 62, wherein said step of forming an undoped second oxide comprises forming a second oxide that is thicker over said gate than lateral to said gate, and wherein said second oxide is thicker over said substrate than lateral to said gate.

65. (Original) The method of claim 64, wherein said step of forming an undoped second oxide comprises:

depositing 500 to 1000 Angstroms of said second oxide over said gate;

depositing 500 to 1000 Angstroms of said second oxide over said substrate; and

depositing 0 to 50 Angstroms of said second oxide lateral to said gate.

66. (Original) A method of depositing an interlayer dielectric, comprising:

providing a first level of a semiconductor device, said first level defining a topography and comprising insulation;

depositing BSG onto discrete portions of said topography, said BSG having a dielectric constant of at most 3; and

providing a second level of said semiconductor device over said BSG.

67. (Original) The method in claim 66, wherein said step of depositing BSG comprises:

depositing glass onto said topography, said depositing resulting in a planar surface of said glass; and

lowering a dielectric constant of said glass.

68. (Original) The method in claim 67, wherein said step of depositing glass comprises:

flowing a silicon oxide precursor over said topography; and

hardening said precursor into a silicon oxide.

69. (Original) The method in claim 68, wherein said step of lowering a dielectric constant of said glass comprises doping said silicon oxide with boron.

70. (Original) The method in claim 69, wherein said step of providing a first level of a semiconductor device comprises providing a first level further comprising at least one conductive structure.

71. (Original) A method of processing a portion of a device including a higher horizontal surface, a lower horizontal surface, and a non-horizontal surface, said method comprising:

providing an oxide in a non-conformal manner over said higher horizontal surface, said lower horizontal surface, and said non-horizontal surface; and

introducing an impurity into said oxide.

72. (Original) The method in claim 71, wherein said step of providing an oxide in a non-conformal manner comprises providing an oxide having a first thickness on said higher horizontal surface, a second thickness on said lower horizontal surface, and a third thickness on said non-horizontal surface, wherein said first, second, and third thicknesses are different.

73. (Original) The method in claim 72, wherein said step of providing an oxide comprises providing an oxide having a first thickness greater than said second thickness.

74. (Original) The method in claim 72, wherein said step of providing an oxide comprises providing an oxide having a second thickness greater than said first thickness.

75. (Original) The method in claim 74, wherein said step of providing an oxide in a non-conformal manner comprises reacting methylsilane and hydrogen peroxide in an environment including a substrate having a temperature of about 20°C.

76. (Original) The method in claim 75, wherein said step of providing an oxide comprises providing an oxide over a non-horizontal surface connecting said higher horizontal surface to said lower horizontal surface.

77. (Original) A method of forming a doped oxide over a substrate, comprising:

reacting a methylsilane with hydrogen peroxide proximate said substrate;

forming an oxide from a product of said methylsilane and said hydrogen peroxide;

and

introducing a dopant into said oxide.

78. (Original) The method in claim 77, wherein said reacting step comprises reacting said hydrogen peroxide with a selection comprising dimethylsilane, trimethylsilane, tetramethylsilane, pentamethyldisilane, and combinations thereof.

Claims 79-88 (Cancelled).